SILICON PROCESSING
FOR
THE VLSI ERA

VOLUME 1:
PROCESS TECHNOLOGY
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STANLEY WOLF Ph.D.
RICHARD N. TAUBER Ph.D.

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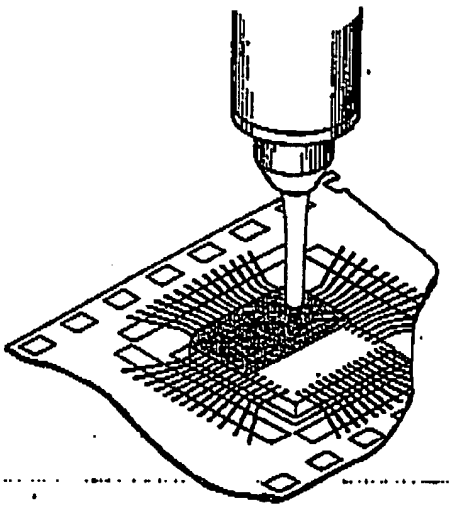

Fig. 17-13 TAB encapsulation.[2] Reprinted with permission of Van Nostrand Reinhold.

wire bonds) TAB also offers a lower profile, which makes TAB applicable for smart-cards, watches, read/write head circuitry, flash memory modules, and the like. The disadvantages of TAB are: 1) it requires a special tape design for each different chip design; 2) there is less infrastructure to provide testability of packaged TAB parts and for mounting the packaged TAB parts to the next levels of packaging; and 3) higher cost compared to wire bonding.

17.5.4 Flip-Chip Bonding

In *flip-chip technologies* solder bumps are fabricated directly on the Al bonding pads of the chip. The chip is then flipped face down and aligned to the package or substrate. The bumps are

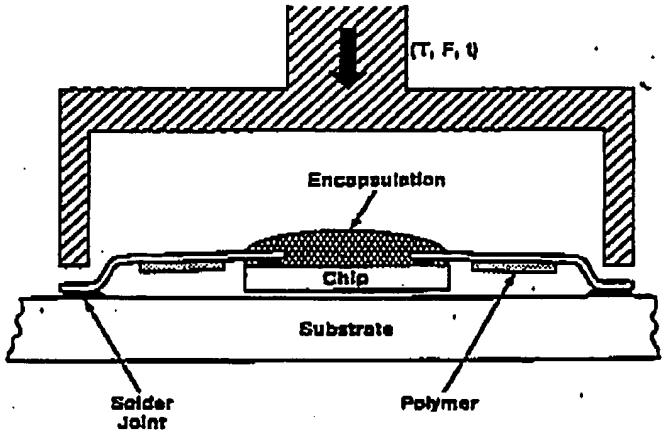

Fig. 17-14 TAB outer lead bonding.[2] Reprinted with permission of Van Nostrand Reinhold.

bonded directly (and all at once) to the package (or substrate) pads by reflowing the solder bumps. The process was introduced by IBM in 1964, and they called it C4 for *controlled collapse chip connection.*[14] The advantages of flip-chip bonding are: 1) the entire chip surface can be covered with solder bumps (making it an *area-array interconnect*). In other words, bonding locations are not limited to the chip perimeter, thus more I/O capability is provided than by a perimeter-interconnect on a die with the same size; and 2) the very short lengths of the chip-to-package interconnect paths minimizes their inductance.

As in TAB, the bumps are formed while the chip is still in wafer form. The bump formation process represents an added expense to overall wafer fabrication cost. However, since this process eliminates the cost of wire bonding, other production costs are reduced. Furthermore, the bump metallurgy reveals the area over the bonding pads that otherwise remains open after wire bonding. Thus, flip-chip technology hermetically seals the chip without the need for a package. This attribute is being exploited for so-called "packageless" attachment of die to substrates (discussed in Section 17.10.2).

The solder bumps most widely used to attach chips to alumina ceramic substrates have been high lead solders, especially 95 Pb:5 Sn. This solder melts at the relatively high temperature of 315°C, which permits other lower-melting-point solders to be used in subsequent module-to-card, or card-to-board packaging level processes without remelting the flip-chip bonds. A multilayer film of metal (e.g., Cr-Cu-Au) is sandwiched between the Al chip pad and the solder bump to prevent the solder from interdiffusing into the Al. The Cr-Cu-Au film forms a cap over each of the Al bonding pads, and the size of each cap is also restricted by sequentially evaporating the Cr-Cu-Au film through a mask (Fig. 17-15*a*). The Pb:Sn is next evaporated onto the chip, again through a mask. The local area of each Pb:Sn layer is slightly larger than the area of the cap. Heating the wafer in an H_2 ambient at 350°C melts these localized Pb:Sn layers. The surface tension of the liquid solder causes the film to recede from the oxide surface, and to form a solder ball on top of the Cr-Cu-Au cap. The diameter of the base of these spherical bumps is determined by the dimension of the Cr-Cu-Au cap. This process is called *ball-limiting metallization* or BLM (see Fig. 17-16). Note that bumps made of conductive epoxy, which allow

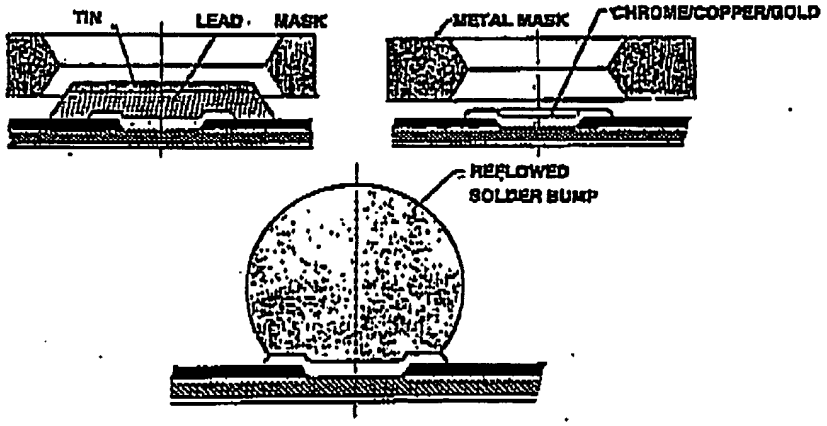

Fig. 17-15 Fabrication of solder bumps for C4 technology.[15] © ISHM 1974.

lower temperature processing than solder bumping, have been pioneered by the Polymer Flip-Chip Corp.[16,17]

Following the reflow of the solder bumps that connect the chip to the substrate, an underfill adhesive is formed between the chip and the substrate.[18] Such underfilling is necessary to reduce the stress on the solder bumps during temperature cycling. When the underfill adhesive is present, it shoulders a large fraction of the stress burden, and the stress on the bumps is significantly reduced. This decreases their tendency to fail through solder-bump stress fatigue.

The underfill adhesive (an epoxy or polyimide) is dispensed as a bead along the perimeter of the bump-attached chip. The chip is heated to 70–100°C and this lowers the viscosity of the underfill epoxy so that capillary force wicks it into the space underneath the die. Once flowed into place, the epoxy is cured to its solid form by an additional heat-curing step.

The term "flip chip" refers only to the method of attachment. No indication is made about what the chip is attached to. That is, if the chip is attached to a package it is called *flip-chip in package* (FCIP) and this method applies to single chip packages and multi-chip modules (MCMs). FCIP is used when the electrical performance of wire bonds is inadequate or when the number of I/Os is too large for wire bonding. Use of FCIP together with a ball-grid array package (see Sect. 17-10) would represent a packaged chip with a very large I/O count. For example, the Intel Pentium II microprocessor is put into plastic and ceramic BGAs and MCMs with flip-chip attach. *Direct chip attach* (DCA) refers to the direct attachment of a chip to a printed circuit board (also called *flip-chip on board*). *Flip-chip DCA* (FC-DCA) bypasses the attachment of the chip to the package.

Flip-chip attachment, however, has some limitations, including the following:

1. The infrastructure for manufacturing, testing, and handling flip-chips from semiconductor vendors by 1998 was not yet mature. Yet, forecasts were that by 2001 the number of chips requiring FC bumping will have increased to more than 2.5 billion. Furthermore, by 1998, flip-chip foundries were beginning to emerge.
2. A lack of standards exists for these procedures, due to the limited adoption of the flip-chip technology by the late 1990's.

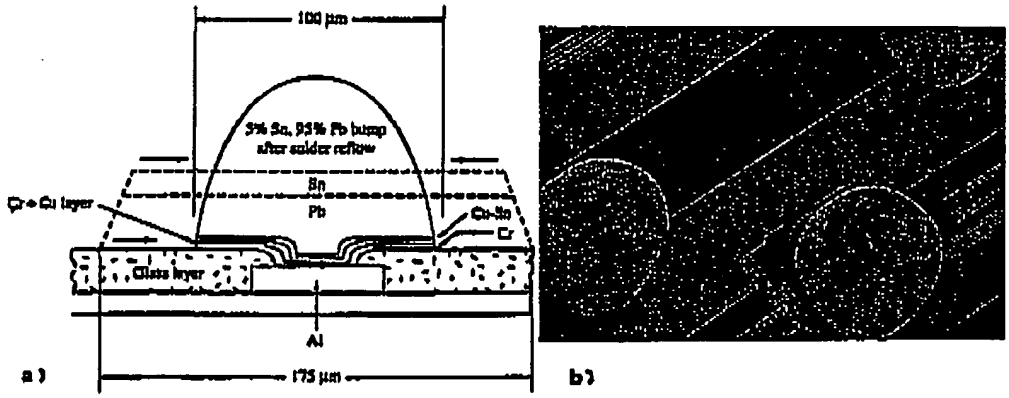

Fig. 17-18 (a) Cross section of a solder bump used in flip-chip technologies and the deformation caused by reflow-soldering operations; (b) SEM view of the C4 solder bumps on a chip.[14] Reprinted with permission of IBM Corporation.

3. Some of the manufacturing issues are also difficult. For example, visual verification of bump placement is not easy, making die placement accuracy very important. Thermal cycle fatigue of the solder joints is also a problem, especially if an underfill material is not used. The viscosity of the underfill epoxy material, however, changes with time, making the under-fill wicking process vary over the space of a day or shift. Another problem is that most ordinary Pb solders contain trace quantities of radioactive elements (i.e., which emit alpha particles that can cause soft errors in memory circuits). Solders made from lead that emits low levels of alpha particles are available for applications that cannot tolerate high soft error rates.

17.6 INTRODUCTION TO CHIP PACKAGES

Integrated circuit chips (or die) are usually encapsulated in an IC package prior to their being installed into electronic systems.[19] IC packages perform four key functions:

1. They provide a sturdy set of leads that allow an IC to be connected to the system in which it will operate. These leads, however, should not significantly degrade the performance of the chip housed by the package.
2. They provide physical protection for the chip against breakage or scratching.
3. They provide environmental protection for the chip against damage from chemicals, moisture, or gases.
4. They dissipate the heat generated by the chip during operation. Chips generating large quantities of heat require additional measures to be incorporated into the package design.

In order to achieve the above objectives, packages are designed to have the following characteristics: 1) low lead capacitance and inductance; 2) material compatibility; 3) good thermal conductivity; 4) good hermetic integrity; 5) ease of manufacture; 6) low cost; and 7) stress levels that will not harm the chip or package. ICs in packages are also easier to handle and test than bare die. They make it easier to compensate for the mismatches in coefficients of thermal expansion among the materials used in the construction of electronic systems. Chip packages, however, also impact the cost, reliability, and sometimes even the performance of the IC (and maybe even the system in which the IC is being used). Reduction in the prices of electronic systems have primarily been driven by the shrinkage of the IC devices themselves, but improvements in packaging have also helped decrease these costs. Packaging cost is important because it can account for a significant fraction of the total cost of the packaged IC. This cost, as measured by cost per pin, has increased from about 1 cent ($US) per pin in small-scale and medium-scale ICs (SSI and MSI), to about 10 cents per pin for ULSI. For ULSI devices in ceramic packages, the package cost may exceed the chip cost by more than 2 times.

In the upcoming sections IC packages will be described. The discussion begins by comparing hermetic (ceramic) and non-hermetic (plastic) packages. Then various IC package types (i.e., through-hole versus surface mount, and specific package configurations) will be analyzed. Finally, so-called "packageless" techniques for ICs are described.

IC package technology is generally divided into two categories, namely: *hermetic* and *non-hermetic* (i.e., plastic) packages. In hermetic packages the chip is housed in an environment isolated from the external world by a vacuum-tight enclosure. The package material is usually ceramic-based, and the two most widely used hermetic-package types are *ceramic packages* and *glass-sealed refractory (cerdip) packages*. Such packages are used in high-reliability